

Performance degradation of SRAM cells due to NBTI effects

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Abstract—SRAM cells play an important role in today's world and the impact they have on memory designs is tremendous. Different types of SRAM cells have been designed till date but consistent efforts are still being made to look out for ways to improve their performance. One such thing that affects the performance of the SRAM cells is the NBTI (Negative Bias Temperature Instability). This paper uses a simple 6T SRAM cell to see what exactly NBTI does to these cells and what happens as a result of the same. This paper explains more about what NBTI actually is, how does it arise, how do they change the device behavior or characteristics and what exactly happens to these SRAM cells on account of this effect. Also, apart from the effect of the NBTI on SRAM cells, this paper also shows the leakage current that persists in the SRAM cell while the entire circuit is switched off (standby mode).

Index Terms—6T SRAM cell, Leakage current, NBTI (Negative Bias Temperature Instability)

I. INTRODUCTION

Technology is known for its allurements and we all know how much it bothers us when it comes to new inventions and developments in any field of interest. It gives a great deal of joy when we get to know and use that technology in real. That is how we got familiar with devices like laptop from personal computers, smart phones from normal cellular phones, Bluetooth devices, Wi-Fi routers, NFC (Near Field Communication) etc. All those we thought were not possible are now actually those that we use in real time in life. That is what technology does and the backbone for all these developments I would say is the MOSFET device that has been in use since ages.

II. INTRODUCTION TO MOSFETS

MOSFET is all that comes to our mind when we recall the developments made in the field of solid state electronics and VLSI design. When we say MOSFET, the immediate aspect that comes to our mind is its different application areas and the different type of MOSFETS used in real time applications. These can be characterized in many ways from application point of view. But by delving deeper into the physical properties of the MOSFET devices we get to know how actually devices are fabricated and designed for use in real time applications.

Many properties affect the design and use of the MOSFETS such as scaling, reliability, speed, performance etc. These when noted in general gives you a wider perspective of the devices that use this so called MOSFET

but what exactly they mean are very intrinsic to the MOSFET device itself.

We all know that MOSFETs are in use for a long time in making efficient processors but at the same time it is also important to know that scaling is something that has been in great discussions till date. Scaling means to size the transistors, precisely the transistors' parameters like width, length, threshold voltage, supply voltage etc. Scaling happens as and when technology improves and the way the MOSFETs are being fabricated also differs from time to time. This paper does not go in detail about scaling but explains what scaling can cause to the SRAM cells, how NBTI occurs in MOSFET devices and the impact it has on the SRAM cells.

III. DIFFERENT PARAMETERS ASSOCIATED WITH A PMOSFET DEVICE

The PMOSFET device basically consists of an n-type substrate (bulk-means that the majority charge carriers are electrons) with p-type (meaning that the majority charge carriers are holes) source and drain terminals on the either sides [1, 2, 5]. On top of the bulk, lies the oxide layer (silicon di-oxide) on top which is the gate terminal. This constitutes the PMOSFET. Basically in order to make the MOSFET function, we supply a small amount of voltage at the gate terminal. When this voltage at the gate exceeds a particular threshold value, it conducts meaning that the electrons are ready to move, make some collisions between them and the silicon lattice atoms to generate the drive current [8, 11]. But this is where NBTI comes into play. Fig. 1 shows a clear picture of a PMOSFET and a MOSFET device [4, 5, 7].

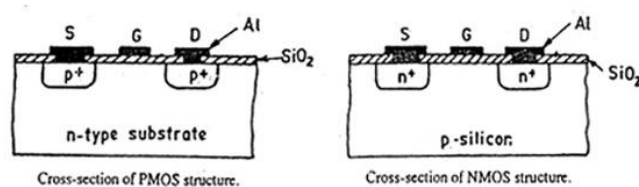


Fig. 1 Structure of a PMOSFET and a NMOSFET device

The fabrication process is performed in such a way that the silicon wafer is exposed to a process called hydrogenation immediately following the oxidation process where the oxide layer is formed [10]. This hydrogenation process generates hydrogen atoms that form weak bonds with the silicon atoms near the surface between the bulk and the oxide layer. These are weak bonds because they can be broken easily upon bombardment of a charged particle [11].

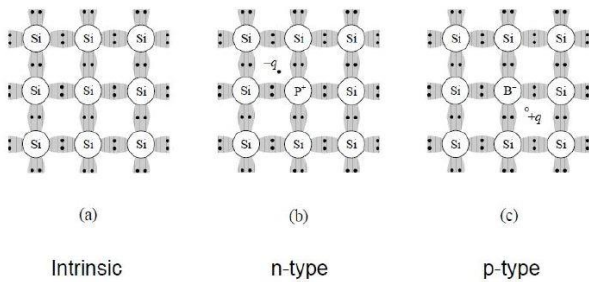


Fig. 2 Lattice space consisting of Si atoms in (a) Intrinsic Silicon, (b) n-type Silicon and (c) p-type Silicon

When a negative bias is applied to the PMOSFET at strong inversion the p-type source and drain terminals acting as the reservoirs contribute the majority charge carriers (holes) to the bulk silicon near the surface (interface) between the bulk and the oxide layer. Now what happens is that a layer or channel forms between the bulk and the oxide near the surface and it is called as the inversion layer [13, 17]. It is so called as inversion layer because the layer that is formed consists of holes in contrast to the bulk that holds electrons.

This inversion is more widely called as inversion channel and it basically spans from the source terminal to the drain terminal. This channel length from the source to the drain is called the channel length when it comes to device parameters of MOSFETs [14, 19, 20]. Fig. 2 gives a reference to where exactly the inversion channel is formed in a MOSFET device.

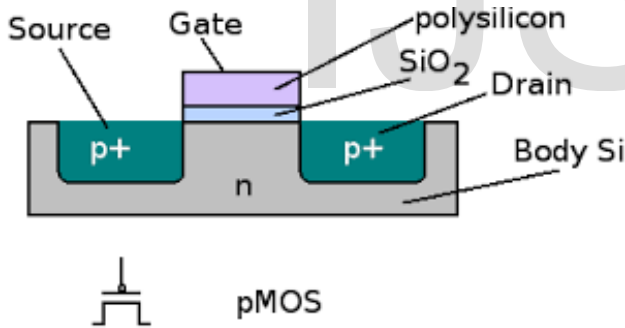


Fig. 3 General MOSFET device showing its inversion channel

Now, since this happens near the surface of the MOSFET, the surface is said to be at a higher potential because it took a lot of energy for the inversion to take place than that for the bulk. Thus, at strong inversion we say that the surface potential is always higher. This can also be explained in the form of band bending i.e. how far the bands such as conduction band, valence band, Fermi level etc. bend with respect to the strong inversion that takes place [20, 21].

The equation that is used to calculate the voltage supplied to the gate terminal is

$$V_g = V_{fb} + 2\psi_B + V_{ox} \tag{1}$$

Where

V_g is the voltage applied at the gate.

V_{fb} is the flat band voltage.

ψ_B is the bulk potential.

V_{ox} is the potential across the oxide layer.

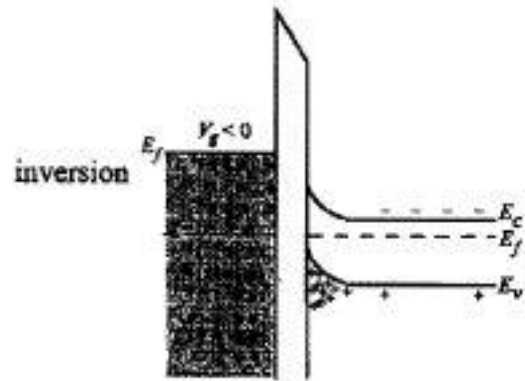


Fig. 4 A broader perspective of band bending in a PMOSFET device during strong inversion

So it is with this equation that we actually determine the gate voltage while knowing the flat band voltage, voltage across the oxide layer and the surface potential. While we need these values to determine the gate voltage, it is said that the flat band voltage and the surface potential remain constant for a particular device and dopant concentration.

The flat band voltage has a direct dependence on the metal work function that is actually used in the device and so it remains constant for a particular combination of metal and substrate. While flat band voltage depends on the work function, on the other side we have the surface potential to be dependent on the bulk potential given by the equation

$$\psi_S = 2\psi_B = (2KT/q) * \ln (N_a/n_i) \tag{2}$$

Where

ψ_S is the surface potential.

ψ_B is the bulk potential.

K is the Boltzmann constant.

T is the temperature of operation.

q is the charge of an electron.

N_a is the doping concentration.

n_i is the intrinsic carrier concentration.

The flat band voltage is said to be constant because it depends on the work function of the metal in use and that work function remains constant for a particular metal. On the other hand, the surface potential is said to be constant because the bulk potential depends on a number of parameters like temperature, charge of an electron etc. [17, 19] that are always constant under consideration.

Also, the doping concentration remains constant and does not change over time. The intrinsic carrier concentration is said to be a constant value because for intrinsic silicon the number of electrons remains the same.

Fig. 4 and equations (1) and (2) as referenced from 'Fundamentals of MODERN VLSI DEVICES, Taur & Ning, Cambridge Univ. Press, 1998. (ISBN 0 521 55056 4); 2nd ed., 2009'

Intrinsic carrier concentration is nothing but the carrier concentration of the silicon in its purest form [6, 7].

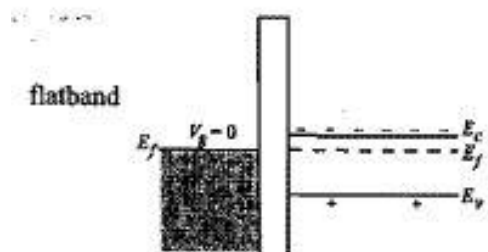


Fig. 5 Flat Band condition for a PMOSFET device

IV. NBTI

So far we have seen what a flat band voltage is and what a strong inversion does in the form of band bending. Let us now focus them in detail. Negative Bias Temperature Instability has been an issue in the semiconductor industry for quite a long time and its effects have also been into research works by many to determine was to eradicate it.

NBTI occurs on a PMOSFET device when a negative bias is supplied. Upon application of a negative bias, we saw that an inversion channel forms near the surface between the oxide layer and the substrate consisting of holes. Now these high energy holes in the inversion layer interact with the weak Si-H bonds and tend to break them apart [8, 9, 15]. They break down easily because they are weak in nature and cannot withstand the bombardment of the high energy holes in the inversion layer.

Once the hydrogen atoms are separated from the silicon atoms, they tend to move towards the oxide layer and get accumulated there. In this process however, not all but few of the hydrogen atoms get accumulated at the interface and act as defects. Now these defects trap the hydrogen atoms at the surface. This is called as the interface trap [15, 16, 20]. This interface trap has significant effects on the device parameters but this paper does not focus more on the trapping but on the aftermath.

These hydrogen atoms that get accumulated in the oxide layer actually contribute to the overall oxide thickness and the equivalent charge contained in the oxide layer [20, 21]. Because of this increase in the oxide thickness, the overall oxide capacitance get reduced by the following relation.

$$C_{ox} = E_{ox}/T_{ox} \quad (3)$$

This decrease in the oxide capacitance in turn increases the voltage across the oxide layer. Not just the decrease in capacitance that causes this voltage to increase but also the accumulation of charge due to the hydrogen atoms in the oxide layer. Hence, we can say that the equivalent charge in the oxide layer increases. This combination of decreased capacitance and increased oxide charge increases the voltage across the oxide layer.

$$V_{ox} = Q_{ox}/C_{ox} \quad (4)$$

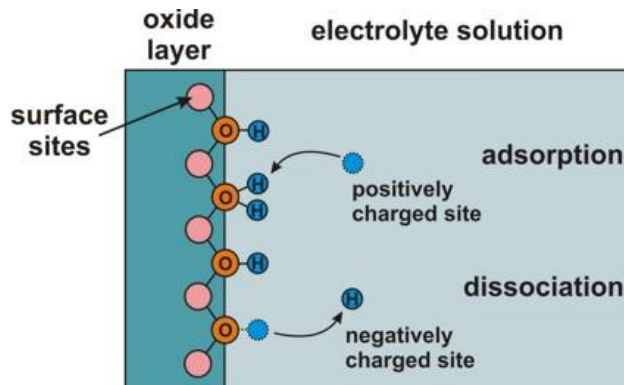


Fig. 6 Interface trap formation due to the broken H atoms

This increase in the voltage across the oxide layer increases the threshold voltage of the MOSFET device followed by the equation

$$V_t = V_{fb} + 2\psi_B + V_{ox} \quad (5)$$

Where

V_t is the threshold voltage.

V_{fb} is the flat band voltage.

ψ_B is the bulk potential.

V_{ox} is the potential across the oxide layer.

With the above mentioned increase in the voltage across the oxide layer, while keeping the flat band voltage and the bulk potential constant, we can see that there is an increase in the threshold voltage of the MOSFET device. This increase in the threshold voltage and the decrease in the oxide capacitance in turn decrease the drive current followed by the equation

$$I_d = (1/2) * (\mu_n C_{ox} (W/L) (V_{GS} - V_{th})^2) \quad (6)$$

Where

V_{th} is the threshold voltage.

C_{ox} is the oxide capacitance.

μ_n is the mobility of the charge carriers.

V_{GS} is the gate to source voltage.

I_d is the drain current or the drive current.

W/L is the width to length ratio of the MOSFET device.

From this equation we can see that while we keep the value of the other parameters like mobility, width to length ratio, gate to source voltage etc. constant, as the threshold voltage increases and the oxide capacitance decreases, the effective drain current (drive current) decreases. This decrease in the drain current in turn affects the performance of the device as a whole.

Fig. 5 and equations (3), (4), (5) and (6) as referenced from 'Fundamentals of MODERN VLSI DEVICES, Taur & Ning, Cambridge Univ.Press, 1998. (ISBN 0 521 55056 4); 2nd ed., 2009'

This is because the drain current of the transistors are responsible for the read and write operation of the SRAM cells that will be discussed in the next section.

V. BASIC 6T SRAM CELL

A basic 6T SRAM cell consists of a pair of inverters cross-coupled to each other while also connected to pass transistors acting as the access transistors. They are called as access transistors because they provide access to the cross-coupled inverters for the read and write operations. These 6 transistors form the 6T SRAM cell. Now, with regards to the read and write operation we have 3 different lines connecting the entire circuit. They are the 'write' line, 'bit' line and the 'bit-bar' line. It is with the help of these three lines that we actually carry out the three different modes of operation of the SRAM cells. The three different modes of operation of the SRAM cells are 'Standby' mode, 'Read' mode and the 'Write' mode.

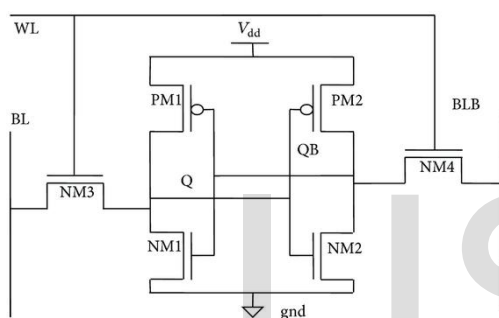


Fig. 7 Basic 6T SRAM cell

1. Standby Mode

Standby mode is a mode where there is no cell operation being performed i.e. a state in which the cell is idle. This happens when the value stored at 'WL' is a '0'. This means that the access transistors 'NM3' and 'NM4' are separated from the cross-coupled inverters. So, therefore even there is a value stored at the 'BL' or 'BLB' lines, the entire circuit is switched off and no operation takes place. It is also in this mode that leakage current or leakage power of the SRAM cell is determined as the supply voltage is still ON.

2. Read Mode

Read mode is when you make the 'WL' go HIGH ('1') in order to switch ON the access transistors 'NM3', 'NM4' and then fetch the values stored at the internal nodes 'Q' and 'QB' with the help of the bit lines 'BL' and 'BLB' respectively. When the access transistors are turned ON, it means that the bit lines are now connected to the cross-coupled inverters. Say for instance the value stored at node 'Q' is a HIGH ('1') and the value stored at the node 'QB' is a LOW ('0'). Then the bit line 'BLB' discharges and the value stored at node 'Q' is read out with the help of the bit line 'BL'.

3. Write Mode

In this mode you keep the 'WL' line HIGH ('1') and then charge either of the bit lines to a HIGH ('1'). So, if you want to write a HIGH ('1') say, you make the bit line 'BL' go HIGH ('1') and the other bit line 'BLB' go LOW ('0'). Now, since the access transistors are ON, the bit lines get connected to the cross-coupled inverters and the value stored at the bit line 'BL' is transferred to the cross-coupled inverters. Now you can make the 'WL' go LOW ('0'). This way your SRAM will hold the written data as long as the next write operation is performed wherein the previously stored value is overwritten.

VI. EFFECTS OF NBTI ON 6T SRAM CELL

With respect to the design of a basic 6T SRAM cell as depicted in Fig. 7, when there is a value '0' stored at the node 'Q' it means that the input the PMOS transistor 'PM2' is a LOW ('0'). Thus, the transistor is said to undergo NBTI. To extend this to NMOS transistor, it is the transistor 'NM1' that undergoes PBTI just similar to PMOS undergoing NBTI.

So, during the read operation, when we need to read the value from the bit line 'BL' and the value stored at the node 'Q' is a LOW ('0'), it's the read stability of the SRAM cell that gets affected as the PMOS transistor 'PM2' undergoes NBTI. Similarly, if the node 'QB' is holding a value LOW ('0') and if we are supposed to read the values from the bit line 'BLB' then again we face the NBTI effect on the PMOS transistor 'PM1' and a similar effect of PBTI on the NMOS transistor 'NM2'. As such we have the read stability of the SRAM cell being affected due to this effect of NBTI [22, 24].

Also, if we have to write a LOW ('0') to the SRAM cell, we hold the value of '0' on the bit line 'BL' or 'BLB'. Again we have the PMOS transistors 'PM2' and 'PM1' undergoing the effect of NBTI respectively. Thus we can say that the cell's write ability is affected due to NBTI. However, in both the read and the write cycles we have the 'WL' line to hold a value of '1' [22, 24].

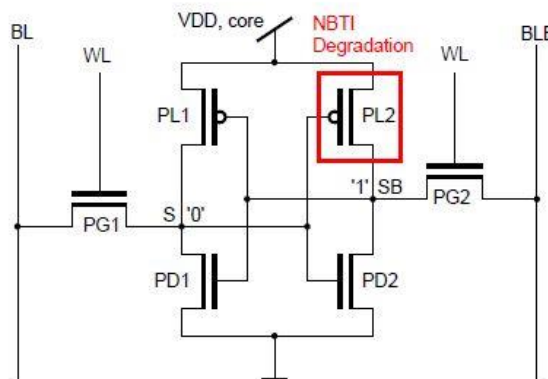


Fig. 8 NBTI effect on a PMOS transistor in a 6T SRAM cell

Since the drive current of the transistors are affected due to the effects of NBTI and PBTI, the overall cell performance is disturbed and thus the SRAM cell does

not behave as intended. The speed of operation is greatly influenced by the drive current i.e. if the drive current is more the cell operates faster and if the drive current is less the cell operation is slower.

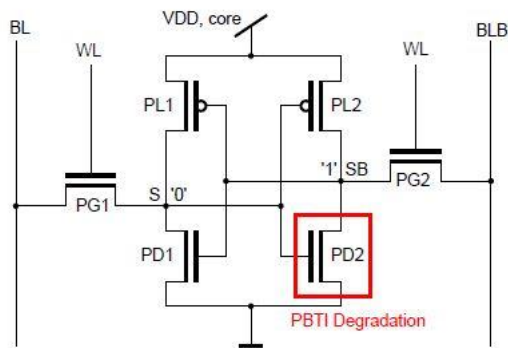


Fig. 9 PBTI effect on a NMOS transistor in a 6T SRAM cell

NBTI reduces the speed of the cell operation and thus make the SRAM cells appear slower to us. Since speed is one of the very important factors for any memory cell, ideally NBTI plays a very significant role in the performance of the SRAM cells [21, 25, 26].

VII. LEAKAGE CURRENT IN A 6T SRAM CELL

Leakage current is the amount of current that flows through any circuit when it is completely idle or not functioning. This means that the supply voltage is still ON even though the circuit remains idle (isolated from any operation). As mentioned, leakage is one of the key factors that any MOSFET device faces when it comes to reliability. Leakage causes the device to perform lesser than expected as time passes by and in turn affects the performance of the devices on a broader span.

Leakage current and hence the leakage power is normally determined for any circuit that is designed so that different methods can be implemented to overcome. It is a good practice to keep the leakage current as small as possible for efficient functioning of the circuit and better reliability.

As far as 6T SRAM cells are considered, there is a small amount of current that flows in the circuit from the supply to the ground when the cross-coupled inverters are completely turned OFF by isolating them from the access transistors. This is done by turning OFF the access transistors by making the 'WL' line go LOW ('0').

Hence the bit lines 'BL' and 'BLB' are disconnected from the cell and no operation takes place. In short, the SRAM cell is considered to be in the 'Standby' mode. Leakage current is also one of the key factors affecting the performance of the SRAM cells as it is the current that flows in the circuit when the cell is under isolation [14, 23, 27].

VIII. DESIGN AND SIMULATION

This paper focused on designing a basic 6T SRAM cell to determine its read stability and write ability. Cadence was used to design the SRAM structure and the technology that was used for this design was 45nm technology.

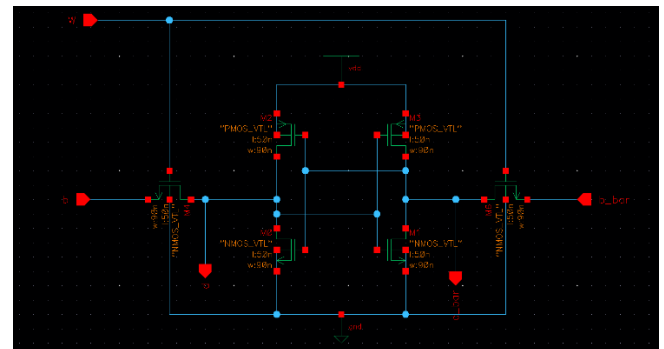


Fig. 10 Basic schematic of a 6T SRAM cell

Fig. 10 gives us the schematic representation of a 6T SRAM cell with which we determine the basic operation modes of the SRAM cell namely the 'Standby' mode, 'Read' mode and the 'Write' mode. The waveforms pertaining to the read and write operations of the 6T SRAM cell is depicted in Fig. 11.

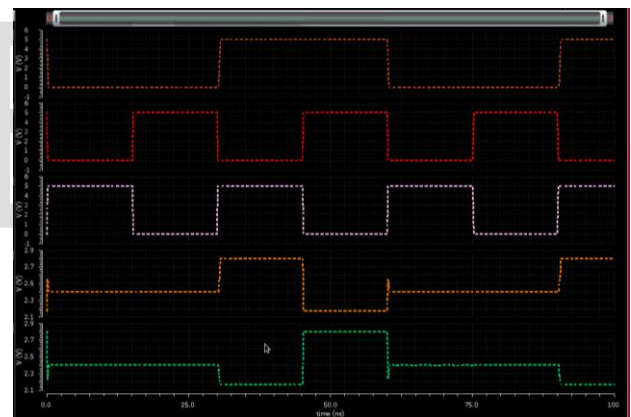


Fig. 11 Waveforms for read and write operation of the 6T SRAM cell

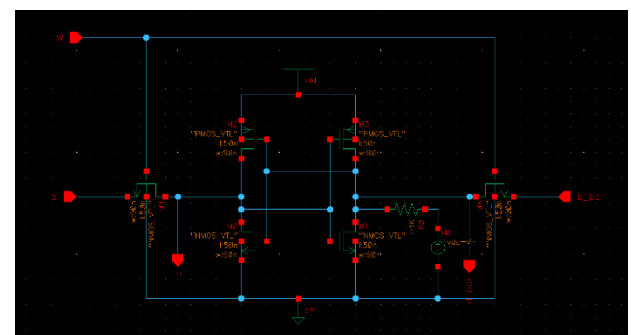


Fig. 12 Schematic representation of a 6T SRAM cell to determine the read and write current

However, the same circuit can be used to determine the read stability and write ability by making a small tweak in the circuit design. An external voltage source is added to one of the internal nodes (either 'Q' or 'QB' from Fig. 7) and then add a resistor in between with a value of 0 Ohms. This

will form a wire that is required to determine the amount of read and write current. The schematic diagram is represented in the Fig. 12.

The waveforms that the schematic in Fig. 12 gives us is shown in Fig. 13 (a) and Fig. 13 (b). These waveforms are used to determine the different parameters associated with the 6T SRAM cell that is in turn used to determine the read and write current.

The parameters that define the read stability and write ability of a 6T SRAM cell are namely the SVN, SINM, WTI and the WTV. The parameter SINM (Static Current Noise Margin) is used to determine the read stability of the SRAM cell while the parameter WTI (Write-Trip Current) defines the voltage required to write the value into the SRAM cell while the bit lines are kept at HIGH ('1'). The SINM corresponds to the read peak current depicted in the Fig. 13 (a) and the WTI corresponds to the write peak current depicted in the Fig. 13 (b).

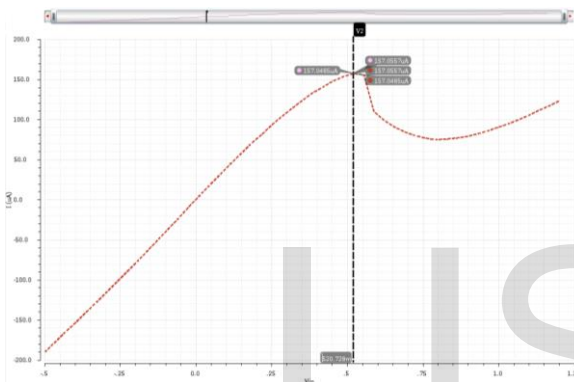


Fig. 13 (a) Waveform representing the read current

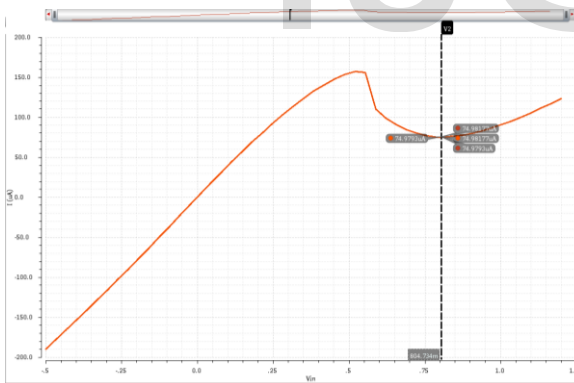


Fig. 13 (b) Waveform representing the write current

The peak current depicted in the Fig. 13 (a) gives us the read current (peak current for read operation) and it is a measure of how far is the SRAM cell stable enough to read the required data with the help of the bit lines while being affected by the NBTI effect.

The peak current depicted in the Fig. 13 (b) gives us the write current (peak current during the write operation) and it is a measure of the ability of the SRAM cell to possibly write the value into the cell while still being affected by the effect of NBTI.

The other parameters are the SVN (Static Voltage Noise Margin) that defines the maximum tolerable noise voltage that the SRAM cell can withstand and the WTV

(Write-Trip Voltage) that defines the voltage required to flip the internal nodes of the SRAM cell while the bit lines are clamped to the power supply. The voltage difference between the two points as depicted in the Fig. 14 (a) and Fig. 14 (b) gives us the SVN and the voltage difference between the two points as depicted in the Fig. 14 (b) and Fig. 14 (c) gives us the WTV.

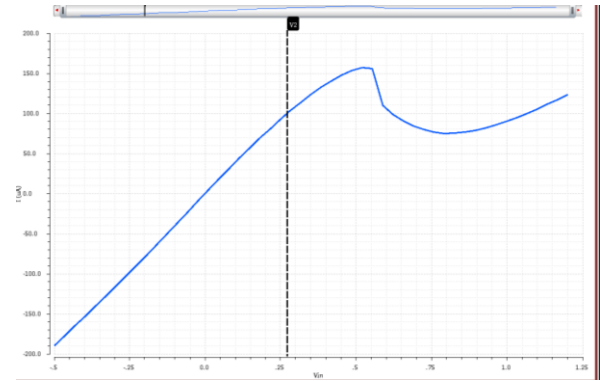


Fig. 14 (a) Waveform showing the first point to determine the SVN

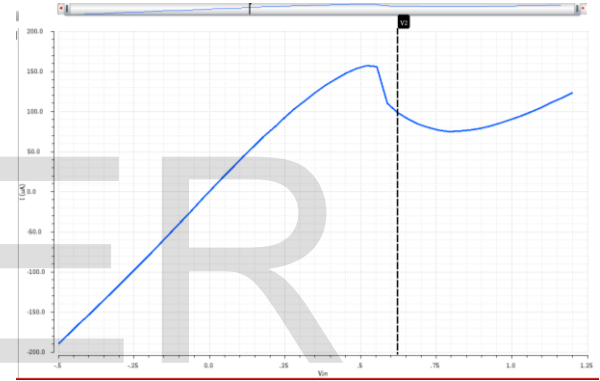


Fig. 14 (b) Waveform showing the second point to determine the SVN which is also the first point to determine the WTV

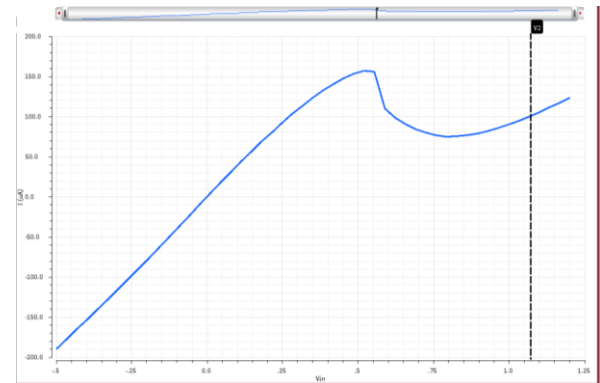


Fig. 14 (c) Waveform showing the second point to determine the WTV

This paper also explains the importance of leakage current that was discussed earlier. However, the basic 6T SRAM cell that was initially designed is used for this purpose except for a single change in the circuit. A resistor with 0 Ohms is added between the NMOS transistors 'NM1'-'NM2' (from Fig. 7) and the ground supply.

This forms the wire that in turn is used to determine the amount of leakage current that flows in the circuit while the cell is not operated at all (ideally in the 'Standby' mode).

For this, the ‘WL’ line is made LOW (‘0’) so that the access transistors are completely detached from the cross-coupled transistors. The schematic representation of the circuit is shown in the Fig. 15 (a).

The waveform that follows the schematic depicted in the Fig. 15 (a) is shown in the Fig. 15 (b) below. The waveform in the Fig. 15 (b) shows the leakage current of the SRAM cell that was designed with respect to the supply voltage. Normally, for a particular supply voltage say 1 V or 3 V or 5 V, we have the leakage current for any circuit to be a constant value. But, this paper shows us how the leakage current varies with respect to a changing supply voltage.

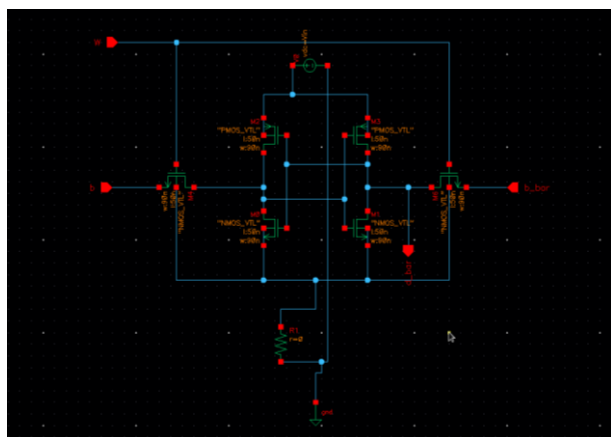


Fig. 15 (a) Schematic representation of the 6T SRAM cell used to determine the leakage current

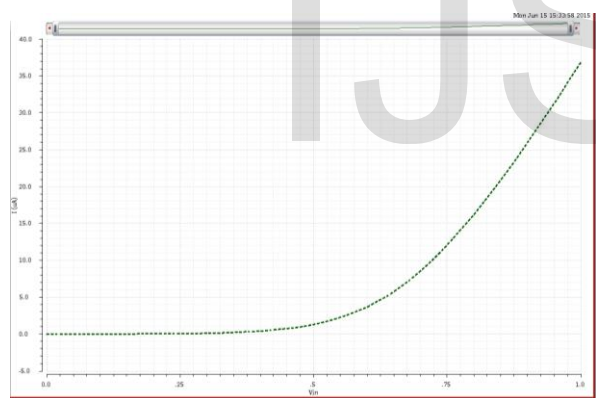


Fig. 15 (b) Leakage current in a 6T SRAM cell

That is, how does the leakage current vary if we sweep down the voltage from 1 V to 0 V. As intended, we did get the leakage current to decrease as expected for decreasing supply voltage from 1V to 0 V.

The amount of read stability and write ability that was achievable using the 6T SRAM cell and 45nm technology is shown in the Table. 1.

| | |
|---|-------------|
| SVNM | 350.518 mV |
| SINM (Read Stability) | 57.0485 μA |
| WTV | 448.8160 mV |
| WTI (Write Ability) | -25.0207 μA |
| Leakage Current (for supply voltage at 1 V) | 37 μA |

Table. 1 Results of the simulation talking about the read stability and the write ability of the 6T SRAM cell along with the leakage current

Where

mV = Milli Volts

μA = Micro Ampere

IX. CONCLUSION

NBTI is a phenomenon that persists in any device that uses transistors (PMOS transistor to be precise). It cannot be avoided because it is something that takes place at the device level and which changes the parameters of the device. This change in the characteristics of the transistors or the device will have effects on the performance in terms of speed, accuracy, efficiency, gain etc. Hence, proper care must be taken to ensure that the device is unaffected by this phenomenon called NBTI.

Constant efforts are being made to analyze the different methods that can be used to lessen the effect of NBTI. It is also said that it is only possible to lessen the effect of NBTI but not completely get rid of it as it is a problem at the device level itself.

There are a number of ways to reduce this effect of NBTI on the SRAM cells by which improved read stability and write ability have been achieved. Hence, it is possible to achieve a higher degree of stability and ability with the different methods on use but quite not possible to completely get rid of this problem.

It is said to be impossible because, even though we analyze and find out a way to completely get rid of this, as and when we scale down the technology and hence the process, it becomes harder for us to determine a better way for the newly invented technology. A number of papers and research works are still being made on finding out ways to lessen or remove the effect of NBTI on SRAM cells using technologies like 90nm, 60nm, 45nm, 32nm etc. However, consistent determination and analytical approach can help us find a better solution to this problem.

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